



MERI College of Engineering & Technology (MERI-CET)

Course- ECE

Session: 2020-2021

Semester: 7th

Department: CSE

Lesson Plan

Name of the faculty : Mr. Neeraj kumar

Discipline : Computer Science and Engineering

Semester : 5th

Subject : **COMPUTER ORGANIZATION & ARCHITECTURE**

Lesson Plan Duration : 15 weeks (From August, 2020 to November 2020)

Work Load (Lecture/ Practical) per week (in hours): Lecture-03, Practical-01

Week	Theory	
	Lecture day	Topic(Including assignment/test)
1 st	1 st	Data representation: Data Types, Complements
	2 nd	Fixed-Point Representation
2 nd	1 st	Conversion of Fractions, Floating-Point Representation
	2 nd	Gray codes, Decimal codes, Alphanumeric codes, Error Detection Codes.
3 rd	1 st	Register Transfer and Micro operations: Register Transfer Language
	2 nd	Register Transfer, Bus and Memory Transfers, Arithmetic Micro operations ,
4 th	1 st	Logic Micro operations, Shift micro operations, Arithmetic Logic Shift Unit.
	2 nd	Basic Computer Organization and Design : Instruction Codes,
5 th	1 st	Computer Registers, Computer Instructions, Timing and Control, Instruction Cycle,
	2 nd	Memory-Reference Instruction, Input-Output Instruction, Complete Computer Description

6 th	1 st	Design of Basic Computer, Design of Accumulator Logic.
	2 nd	Central Processing Unit : General Register Organization,
7 th	1 st	Addressing Modes, Data Transfer and Manipulation, Program Control, RISC, CISC
	2 nd	Pipeline and Vector Processing: Introduction to Parallel Processors
8 th	1 st	Amdahl's Law, Pipelining, Arithmetic Pipeline, Instruction Pipeline
	2 nd	RISC Pipeline, Vector Processing, Array Processors,
9 th	1 st	SIMD Array Processors, Pipeline Hazards.
	2 nd	Input-output Organization : I/O device interface,
10 th	1 st	I/O transfers–program controlled
	2 nd	
11 th	1 st	interrupt driven and DMA, Privileged and Non-Privileged Instructions
	2 nd	Software Interrupts Memory organization : Memory Hierarchy,
12 th	1 st	Main Memory, Auxiliary Memory
	2 nd	Associative Memory, Cache Memory,
13 th	1 st	
	2 nd	Associative Mapping, Direct Mapping
14 th	1 st	Set-Associative Mapping, Writing into Cache.
	2 nd	Cache Initialization, Virtual Memory
15 th	1 st	Stack organization, Instruction Format
	2 nd	
16 th		
17 th	Sessional -II Examination+Activity	

Faculty Signature